Amendments to Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Previously Presented) A circuit, comprising:

a latch;

a storage element coupled to the latch and, during programming of the storage element, the storage element avoids forwarding current from the storage element into the latch; and

a blocking transistor having a source-to-drain path coupled between the storage element and through a programming transistor to an output of the latch.

2. (Original) The circuit as recited in claim 1 is formed using a fabrication process capable of forming sub one-quarter micron features..

3. (Original) The circuit as recited in claim 1 is formed using a fabrication process that avoids additional steps or features needed to accommodate programming voltages that exceed twice the voltages on the latch.

4. (Original) The circuit as recited in claim 1, wherein the latch comprises a pair of cross-coupled inverters.

5. (Original) The circuit as recited in claim 4, further comprising a pair of pass-gate transistors coupled to a data bus to forward true and complementary bit values onto respective ones of the pair of cross-coupled inverters.

6. (Previously Presented) The circuit as recited in claim 1, further comprising a selecting transistor having a gate conductor and a source-to-drain path, and wherein the gate conductor is coupled through a programming transistor to an output of the latch, and the source-to-drain path is coupled between a ground supply and through the blocking transistor to the storage element.

7. (Canceled)

8. (Original) The circuit as recited in claim 1, wherein the storage element comprises a one-time programmable storage element.

9. (Original) The circuit as recited in claim 8, wherein the one-time programmable storage element comprises a dielectric that (i) upon receiving a programming voltage differential across the dielectric a relatively low resistive path will occur to a power supply, and (ii) upon receiving a non-programming voltage differential across the dielectric a relatively high resistive path will occur to the power supply.

10. (Currently Amended) A one-time programmable latching circuit, comprising:

a latch having two pairs of latching transistors connected to form a pair of cross-coupled inverters;

a pair of one-time programmable storage elements coupled to respective outputs of the inverters, wherein the storage elements include a pair of storing transistors having a gate oxide thickness dissimilar from a gate oxide thickness of any of the set of latching transistors; and

a selection circuit that includes a pair of programming transistors with source-to-drain paths coupled between inputs of the pair of cross-coupled ~~transistors~~ inverters and gates of a pair of selecting transistors; and

a margin-testing transistor coupled to vary current from the pair of storage elements read as a voltage differential at an output of the pair of cross-coupled inverters.

11. (Original) The latching circuit as recited in claim 10 is formed using a fabrication process capable of forming sub one-quarter micron features..

12. (Original) The latching circuit as recited in claim 10 is formed using a fabrication process that avoids additional steps or features needed to accommodate programming voltages that exceed twice the voltages on the latch.

13. (Original) The latching circuit as recited in claim 10, further comprising a data bus coupled to inputs of the pair of cross-coupled inverters.

14. (Canceled)

15. (Previously Presented) The latching circuit as recited in claim 10, wherein the programming transistors include a gate terminal adapted to receive a programming voltage and, upon receiving the programming voltage, one of the programming transistors causes programming current to flow from one of the pair of storage elements, through one of the pair of selecting transistors, and directly to a ground supply conductor configured within the latching circuit outside the latch.

16. (Previously Presented) The latching circuit as recited in claim 10, wherein the programming transistors include a gate terminal adapted to receive a programming voltage and, upon receiving the programming voltage, one of the programming transistors causes a binary value on the data bus to be placed on a gate of one of the pair of selecting transistors causing current to flow from one of the pair of storage elements, through one of the pair of selecting transistors, and directly to a ground supply conductor configured within the latching circuit outside the latch.

17. (Original) The latching circuit as recited in claim 10, wherein the latch further comprises a holding transistor coupled between each of the two pair of latching transistors to maintain a latched voltage value on the output of the pair of cross-coupled inverters during times when the holding transistor is activated.

18. (Canceled)

19. (Original) The latching circuit as recited in claim 10, wherein the one-time programmable storage element comprises a dielectric that (i) upon receiving a programming voltage differential across the dielectric a relatively low resistive path will occur to a power supply, and (ii) upon receiving a non-programming voltage differential across the dielectric a relatively high resistive path will occur to the power supply.

20. - 25. (Canceled)